4th International Symposium on
Energy Challenges & Mechanics
- working on small scales

11-13 August 2015
Aberdeen, Scotland, UK

Triple-Gate FinFETs for very high frequency applications

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Accepted for publication on 18th April 2015

CMOS technology has progressed astonishingly during the last decades, due to the successful shrinkage of transistor size, which has been described along the years by the Moore´s Law. Besides, according to the International Technology Roadmap of Semiconductors (ITRS), this development will continue beyond the 10-nm node, which is known as More-Moore technologies (MM). Furthermore, CMOS technology has promoted the possibility to develop novel non-digital applications, this is called the More-than-Moore technologies (MtM).

Under this concept, the integration of passive elements, transducers, RF and power blocks, among others, becomes a priority with the aim of developing complex System-on-Chip (SoC) solutions. In this regard, the communications industry is very demanding because it requires very high frequency, low power consumption, high performance, analog and digital subsystems etc., which becomes a good example of the MM and MtM sharing and industry diversification.

Therefore, the improvement of the RF transistors performance is necessary for the development of the SoCs. Additionally, ITRS establishes that the analog performance of the MOSFETs will continue growing. Thus, Silicon-on-Insulator Triple-Gate FinFETs (SOI-TGFinFETs) are promising candidates to continue the roadmap of analog applications. However, it has been demonstrated that the SOI-TGFinFETs behavior is strongly affected by parasitic series source-drain (R_{sd}) and gate resistances (R_{ge}) and the fringing gate capacitances (C_{gge}).

In this contribution, we show that TG-FinFET geometry optimization leads to an important improvement of the transistor cut-off frequencies, due to the reduction of the parasitics as well as the increment of the intrinsic transconductance. An optimized geometry is attained with 10 and 20 nm for the source/drain extension length (L_{ext}) and the spacing between fins (S_{fin}), respectively. Thanks to this geometry optimization, the cut-off frequencies for SOI-TGFinFETs of 40-nm technology node, can reach values of about 260 and 420 GHz for f_T, and f_{MAX}, respectively. Finally, some tradeoffs, which appear due to the minimization of the parasitics, will be discussed.

Keywords: FinFET; extrinsic resistances and capacitances; cut-off frequency