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CMOS inverter based on Triple-Gate FinFETs for low power electronics

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Silicon-on-Insulator Triple-Gate FinFETs (SOI-TG-FinFETs) have appeared as suitable technology to sustain the downscaling of the CMOS transistors thanks to their superior control of the so-called Short-Channel-Effects (SCE). However, it is well-known that the behavior of those devices is strongly affected by the parasitic parameters, such as series source-drain resistance (R_{sd}), gate resistance (R_{ge}) and gate fringing capacitances (C_{gge}). Under this scenario, proper FinFET optimization might follow specific methodologies in order to cover satisfactorily the application needs.

Very recently, it has been demonstrated that the use of the compact model for symmetric doped double-gate MOSFET (SDDGM) together with geometrical dependent parasitic models allows to reproduce the experimental performance of nanometric n-type TG-FinFET. Thus, the model replicates several characteristics as: (i) transfer and output dc characteristics; (ii) extrinsic transconductance (g_m) and output conductance (g_d); (iii) intrinsic small-signal equivalent circuit parameters (g_{mi}, g_{di}, C_{gdi}, C_{gsi}); (iv) extrinsic small-signal equivalent circuit parameters (R_{se}, R_{de}, R_{ge}, C_{gde}, C_{gse}) and (v) two port behavior (*Z*- and *Y*- parameters).

In this contribution, we analyze, with SDDGM, the CMOS inverter performance based on SOI-TG-FinFETs. The average power consumption and Power-Delay Product (PDP) have been examined. PDP exhibits a strong reduction, as the space between fins (S_{fin}) is reduced, on the other hand, its dependence becomes weak when S_{fin} is smaller than 40 nm. Additionally, PDP has a slight dependence with the source/drain extension length (L_{ext}). Finally, the possibilities of geometry tuning in order to reduce the inverter power consumption will be addressed, with the aim to investigate the potential of the FinFET technology for low power electronics.

Keywords: FinFET; CMOS inverter; Low-Power Electronics